

**DATA STREAM FREQUENCY REDUCTION  
AND/OR PHASE SHIFT**

ABSTRACT OF THE DISCLOSURE

5           A frequency reduction or phase shifting circuit  
has an input receiving an input data stream having an  
input frequency and a representation of desired  
output frequency. A splitter splits the input data  
stream into a plurality of split signals each at a  
10 frequency of the desired output frequency. A  
plurality of catchers identify valid bits of each  
respective split signal. A shifter shifts valid bits  
identified by at least some of the catchers by a  
predetermined number which establishes a de-  
15 serialization level for frequency reduction or phase  
shifting. An output provide an output data stream at  
the desired output frequency.